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NOTICE OF ALLOWANCE AND FEE(S) DUE

77541 7590 12/11/2008

Maryam Imam and LSI Corporation
95 South Market Street
Suite 570
San Jose, CA 95113

EXAMINER	
LEE, CHUN KUAN	
ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 12/11/2008

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,523	02/09/2004	Sam Nemazie	SILICONSTOR-03US	1041

TITLE OF INVENTION: ROUTE AWARE SERIAL ADVANCED TECHNOLOGY ATTACHMENT (SATA) SWITCH

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$755	$300	$0	$1055	03/11/2009

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,523	02/09/2004	Sam Nemazie	SILICONSTOR-03US	1041

TITLE OF INVENTION: ROUTE AWARE SERIAL ADVANCED TECHNOLOGY ATTACHMENT (SATA) SWITCH

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$755	$300	$0	$1055	03/11/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
LEE, CHUN KUAN	2181	710-074000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1_____

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2_____ 3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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LEE, CHUN KUAN	
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2181	

DATE MAILED: 12/11/2008

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 235 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 235 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	10/775,523	NEMAZIE, SAM	
	Examiner	Art Unit	
	Chun-Kuan Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *09/22/2008*.

2. ☒ The allowed claim(s) is/are *1-29*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 5/9/08 & 9/15/08
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Alford W. Kindred/
Supervisory Patent Examiner, Art Unit 2181

DETAILED ACTION

I. ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

1. As required by **M.P.E.P. 609(C)**, the applicant's submissions of the Information Disclosure Statement dated May 09, 2008 and September 15, 2008 are acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P 609 C(2)**, a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

II. EXAMINER'S AMENDMENTS

OPTIONS AVAILABLE TO THE APPLICANT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by **37 CFR § 1.312**. To ensure consideration of such an amendment, it **MUST** be submitted no later than the payment of the issue fee.

AUTHORIZATION FOR THE CORRECTIONS BY THE EXAMINER

3. Authorization for this examiner's amendment was given in a telephone interview with Attorney Maryam Imam, having Reg. No. 38,190, on December 4, 2008. Accordingly, since a complete record of the interview has been incorporated in the instant examiner's amendment, no separate interview summary form is included in the instant office letter **MPEP § 713.04**.

CORRECTIONS MADE IN THE APPLICATION

4. The application has been amended as following:

IN THE CLAIMS:

The below described amendments to the claims are necessary to further clarify the claimed invention.

NOTE: The claims amended by this examiner's amendment have been referred to by their original claim number.

5. In claim 1, "…A switch coupled between a plurality of host units and a device for routing frame information therebetween and comprising:

a. a first serial advanced technology attachment (ATA) port including a first host task file responsive to a non-data frame information structure (FIS) from a first host unit;

b. a second serial ATA port including a second host task file, responsive to a non-data FIS from a second host unit;

c. a third serial ATA port including a device task file responsive to a non-data FIS from a device, the device configured to support command queuing and operative to generate an original queue depth value indicative of the number of commands that the device can queue from either of the first or second host units; and

d. an arbitration and control circuit coupled to said first host task file and said second host task file and said device task file for selecting one of the first host or second host units to concurrently access the device, through the switch, by accepting

non-data FIS, from either of the first or second host units, at any given time, including when the device is not in an idle state and whenever either one of the first or second host units sends non-data FIS to the device and further wherein the non-data FIS of the first and second host units and the device identify which one of the first or second host units is an origin or destination host so that routing of non-data FIS is transparent to the switch thereby reducing the complexity of the design of the switch rendering its manufacturing less expensive, the arbitration and control circuit being responsive to the original queue depth value and operative to alter the original queue depth value to be a queue depth value that is less than the original queue depth value so that each of the first and second host units is assigned less than the number of commands indicated by the original queue depth value but that the total number of commands that can be queued by the first and second host units remains the same as the original queue depth value thereby misrepresenting the original queue depth value to the first and second host units to be less than that which it is thereby preventing commands being lost by an overrun of the original queue depth value by either of the first or second host units ..." should be replaced with

-...A switch coupled between a plurality of host units and a device for routing frame information therebetween and comprising:

a. a first serial advanced technology attachment (SATA) port including a first host task file responsive to a non-data frame information structure (FIS) from a first host unit;

b. a second SATA port including a second host task file, responsive to a non-data FIS from a second host unit;

c. a third SATA port including a device task file responsive to a non-data FIS from a device, the device supports queuing of the non-data FIS sent by the first and second host units and generates an original queue depth value indicative of a number of commands that the device can queue from either of the first or second host units; and

d. an arbitration and control circuit coupled to said first host task file and said second host task file and said device task file for selecting one of the first host or second host units to concurrently access the device, through the switch, by accepting the non-data FIS from either of the first or second host units, at any given time, including when the device is not in an idle state and whenever either one of the first or second host units sends the non-data FIS to the device, and further wherein the non-data FIS of the first and second host units and the device identify which one of the first or second host units is an origin or destination host so that routing of the non-data FIS from the first and second host units and the device is transparent to the switch thereby reducing the complexity of the design of the switch rendering the switch's manufacturing less expensive, the arbitration and control circuit being responsive to the original queue depth value and alters the original queue depth value to be a new queue depth value that is less than the original queue depth value so that each of the first and second host units is assigned less than the number of commands indicated by the original queue depth value but that a total number of commands queued by the first and second host units remains the same as the original queue depth value thereby misrepresenting the original queue depth value to the first and second host units to be less than the original queue depth value thereby preventing the non-data FIS sent by the first and second

host units from being lost by an overrun of the original queue depth value by either of the first or second host units ...-.

6. In claim 4, line 2, "… causes concurrent access …" should be replaced with - … causes the concurrent access …-.

7. In claim 5, "… wherein a bit is used to indicate which host is the origin or destination of the non-data FIS ..." should be replaced with -… wherein a bit is used to indicate either the first or second host unit is the origin or destination of the non-data FIS from either the first host unit, the second host unit or the device ...-.

8. In claim 6, line 2, "… layer 2 ports …" should be replaced with -… layer 4 ports …-.

9. In claim 9, "… A switch comprising:

a. a first serial advanced technology attachment SATA port including a first host task file for connection to a first host unit, said first SATA port responsive to a non-data frame information structure (FIS) from the first host unit;

b. a second SATA port including a second host task file for connection to a second host unit responsive to a non-data FIS from the second host unit;

c. a third SATA port including a device task file responsive to a non-data FIS, for connection to a device, the switch for routing frame information between the first and

second host units and the device, the device operative to support command queuing and having an original queue depth value indicative of the number of commands that the device can queue from either of the first or second host units; and

d. an arbitration and control circuit coupled to said first host task file and said second host task file and said device task file for selecting either the first host unit or the second host unit to concurrently access the device, through the switch, by accepting non-data FIS, from either of the first or second host units, at any given time, including when the device is not in an idle state, when either one of the first or second host units sends non-data FIS to the device,

wherein while one of the first or second host units is coupled to the device, through the switch, the other one of the first or second host units sends non-data FIS to the switch for routing to the device and further wherein the non-data FIS of the first and second host units and the device identify which one of the first or second host units is an origin or destination host so that routing of non-data FIS is transparent to the switch thereby reducing the complexity of the design of the switch rendering its manufacturing less expensive, further wherein the arbitration and control circuit is responsive to the original queue depth value and operative to alter the original queue depth value into a queue depth value that is less than the original queue depth value so that each of the first and second host units is assigned less than the number of commands indicated by the original queue depth value but that the total number of commands that can be queued by the first and second host units remains the same as the original queue depth value thereby misrepresenting the original queue depth value to the first and second

host units to be less that that which it is so as to avoid commands being lost by overrun of the original queue depth value by either of the first or second host units ..." should be replaced with

-... A switch comprising:

a. a first serial advanced technology attachment SATA port including a first host task file for connection to a first host unit, said first SATA port responsive to a non-data frame information structure (FIS) from the first host unit;

b. a second SATA port including a second host task file for connection to a second host unit responsive to a non-data FIS from the second host unit;

c. a third SATA port including a device task file responsive to a non-data FIS from a device, for connection to the device, the switch for routing frame information between the first and second host units and the device, the device supports queuing of the non-data FIS sent by the first and second host units and generates an original queue depth value indicative of a number of commands that the device can queue from either of the first or second host units; and

d. an arbitration and control circuit coupled to said first host task file, said second host task file, and said device task file for selecting either the first host unit or the second host unit to concurrently access the device, through the switch, by accepting the non-data FIS from either of the first or second host units, at any given time, including when the device is not in an idle state, when either one of the first or second host units sends the corresponding non-data FIS to the device,

wherein while one of the first or second host units is coupled to the device, through the switch, the other one of the first or second host units sends the non-data FIS to the switch for routing to the device, and further wherein the non-data FIS from the first and second host units and the device identify which one of the first or second host units is an origin or destination host so that routing of the non-data FIS from the first and second host units and the device is transparent to the switch thereby reducing the complexity of the design of the switch rendering the switch's manufacturing less expensive, further wherein the arbitration and control circuit is responsive to the original queue depth value and alters the original queue depth value into a new queue depth value that is less than the original queue depth value so that each of the first and second host units is assigned less than the number of commands indicated by the original queue depth value but that a total number of commands queued by the first and second host units remains the same as the original queue depth value thereby misrepresenting the original queue depth value to the first and second host units to be less than the original queue depth value so as to avoid the non-data FIS sent by the first and second host units from being lost by overrun of the original queue depth value by either of the first or second host units ...-.

10. In claim 13, line 2, "… concurrent access …" should be replaced with -… the concurrent access …-.

11. In claim 14, "… A switch that is connectable to a first host unit, a second host unit and a device via serial advanced technology attachment (ATA) links, for routing frame information between the first and second host units and the device, said switch comprising:

a. a first serial ATA port, including a first host task file for connection to a first host unit, said first SATA port responsive to a non-data frame information structure (FIS) from the first host unit;

b. a second serial ATA port, including a second host task file for connection to a second host unit, responsive to a non-data FIS from the second host unit;

c. a third serial ATA port including a device task file responsive to a non-data FIS, for connection to a device, the device operative to support command queuing and having an original queue depth value indicative of the number of commands that the device can queue from either of the first or second host units;

d. an arbitration and control circuit coupled to said first host task file and said second host task file and said device task file for selecting one of the first or second host units to concurrently access the device through the switch, by accepting non-data FIS, from either of the first or second host units, at any given time, including when the device is not in an idle state, when either the first or second host units sends non-data FIS to the device, wherein while one of the first or second host units is coupled to the device, the other one of to the first or second host units sends non-data FIS to the switch for routing to the device and further wherein the non-data FIS of the first and second host units and the device identify which one of the first or second host units is

an origin or destination host so that routing of non-data FIS is transparent to the switch thereby reducing the complexity of the design of the switch rendering its manufacturing less expensive,

further wherein, the arbitration and control circuit responsive to the original queue depth value and operative to alter the original queue depth value into a queue depth value that is less than the original queue depth value so that each of the first and second host units is assigned a number of commands that is less than the number of commands indicated by the original queue depth value but that a total number of commands that can be queued by the first and second host units remains the same as the original queue depth value thereby misrepresenting the original queue depth value to the first and second host units to be less thereby preventing commands being lost by an overrun of the original queue depth value by either of the first or second host units ..." should be replaced with

-... A switch that is connectable to a first host unit, a second host unit and a device via serial advanced technology attachment (SATA) links, for routing frame information between the first and second host units and the device, said switch comprising:

a. a first SATA port, including a first host task file for connection to a first host unit, said first SATA port responsive to a non-data frame information structure (FIS) from the first host unit;

b. a second SATA port, including a second host task file for connection to a second host unit, responsive to a non-data FIS from the second host unit;

c. a third SATA port including a device task file responsive to a non-data FIS from a device, for connection to the device, the device supports queuing of the non-data FIS sent by the first and second host units and generates an original queue depth value indicative of a number of commands that the device can queue from either of the first or second host units;

d. an arbitration and control circuit coupled to said first host task file, said second host task file, and said device task file for selecting one of the first or second host units to concurrently access the device through the switch, by accepting the non-data FIS from either of the first or second host units, at any given time, including when the device is not in an idle state, when either the first or second host units sends the non-data FIS to the device,

wherein while one of the first or second host units is coupled to the device, the other one of to the first or second host units sends the non-data FIS to the switch for routing to the device, and further wherein the non-data FIS from the first and second host units and the device identify which one of the first or second host units is an origin or destination host so that routing of the non-data FIS from the first and second host units and the device is transparent to the switch thereby reducing the complexity of the design of the switch rendering the switch's manufacturing less expensive,

further wherein, the arbitration and control circuit responsive to the original queue depth value and alters the original queue depth value into a new queue depth value that is less than the original queue depth value so that each of the first and second host units is assigned a new number of commands that is less than the number of

commands indicated by the original queue depth value but that a total number of commands queued by the first and second host units remains the same as the original queue depth value thereby misrepresenting the original queue depth value to the first and second host units to be less than the original queue depth value thereby preventing the non-data FIS sent by the first and second host units from being lost by an overrun of the original queue depth value by either of the first or second host units ...-.

12. In claim 18, line 2, "… concurrent access …" should be replaced with -… the concurrent access …-.

13. In claim 19, "…A method for communication between multiple host units and a device, through a serial advanced technology attachment (ATA) switch coupled to the multiple host units and the device using serial ATA links routing frame information therebetween comprising:

a. receiving a non-data frame information structure (FIS) through a first serial ATA port, from a first host unit;

b. receiving a non-data FIS, through a second serial ATA port, from a second host unit;

c. receiving a non-data FIS through a third serial ATA port; d. arbitrating between the first and second host units and the device;

e. selecting one of the first or second host units for coupling to the device through the switch when either of the first or second host units sends commands for execution by the device;

f. coupling the device to the selected one of the first or second host units;

g. while the selected one of the first or second host units is coupled to the device, the other one of the first or second host units sending non-data FIS to the switch for routing to the device

during the sending step g., the non-data FIS of the first and second host units and the device identifying which one of the first or second host units is an origin and/or destination host so that routing of non-data FIS is transparent to the switch thereby reducing the complexity of the design of the switch rendering its manufacturing less expensive;

h. intercepting an original queue depth value from the device, the queue depth value being indicative of the number of commands that the device can queue from either of the first or second host units;

i. altering the original queue depth value to be a queue depth value that is less than the original queue depth value so that each of the first and second host units is assigned less than the number of commands indicated by the original queue depth value but that the total number of commands that can be queued b¥ the first and second host units is the same as the original queue depth value thereby avoiding commands being lost by overrun of the original queue depth value ..." should be replaced with

-…A method for communication between multiple host units and a device, through a serial advanced technology attachment (SATA) switch coupled to the multiple host units and the device using serial ATA links routing frame information therebetween comprising:

a. receiving a non-data frame information structure (FIS) through a first SATA port including a first host task file, from a first host unit;

b. receiving a non-data FIS, through a second SATA port including a second host task file, from a second host unit;

c. receiving a non-data FIS through a third SATA port including a device task file;

d. arbitrating by an arbitration and control circuit between the first and second host units and the device;

e. selecting by the arbitration and control circuit one of the first or second host units to concurrently access the device through the switch, by accepting the non-data FIS, through the first and second host task files, from either of the first or second host units, when either of the first or second host units sends the non-data FIS for execution by the device;

f. coupling by the arbitration and control circuit the device to the selected one of the first or second host units;

g. while the selected one of the first or second host units is coupled to the device, the other one of the first or second host units sending the non-data FIS to the switch for routing to the device

during the sending step g., the non-data FIS of the first and second host units and the device identifying which one of the first or second host units is an origin or destination host so that the routing of the non-data FIS from the first and second host units and the device is transparent to the switch thereby reducing the complexity of the design of the switch rendering the switch's manufacturing less expensive;

h. intercepting by the arbitration and control circuit an original queue depth value generated by the device, the queue depth value being indicative of a number of commands that the device can queue from either of the first or second host units;

i. altering the original queue depth value by the arbitration and control circuit to be a new queue depth value that is less than the original queue depth value so that each of the first and second host units is assigned less than the number of commands indicated by the original queue depth value but that a total number of commands queued by the first and second host units remains the same as the original queue depth value thereby misrepresenting the original queue depth value to the first and second host units to be less than the original queue depth value thereby avoiding the non-data FIS sent by the first and second host units from being lost by overrun of the original queue depth value by either of the first or second host units...-.

14. In claim 20, "… further including the steps of transmitting a non-data FIS through the first serial ATA port, non-data FIS through the second serial ATA port, and transmitting a non-data FIS through the third serial ATA port ..." should be replaced with

-… further including the steps of transmitting the non-data FIS through the first SATA port, the non-data FIS through the second SATA port, and transmitting the non-data FIS through the third SATA port ...-.

15. In claim 21, line 1, "… the queue depth value …" should be replaced with -… the new queue depth value …-.

16. In claim 22, line 5, "…a queue depth value that is no more than one-half that reported …" should be replaced with

-… the new queue depth value that is no more than one-half of the original queue depth value that was reported …-.

17. In claim 23, line 2, "… includes the identity …" should be replaced with -… includes identity …-.

18. In claim 24, line 1, "… the queue depth value …" should be replaced with -… the new queue depth value …-.

19. In claim 25, line 5, "…a queue depth value that is no more than one-half that reported …" should be replaced with

-… the new queue depth value that is no more than one-half of the original queue depth value that was reported …-.

20. In claim 26, line 2, "… includes the identity …" should be replaced with -… includes identity …-.

21. In claim 27, line 1, "… the queue depth value …" should be replaced with -… the new queue depth value …-.

22. In claim 28, line 5, "…a queue depth value that is no more than one-half that reported …" should be replaced with

-… the new queue depth value that is no more than one-half of the original queue depth value that was reported …-.

23. In claim 29, line 2, "… includes the identity …" should be replaced with -… includes identity …-.

III. DISTINGUISHING FEATURES RECITED IN THE CLAIMS

ALLOWABLE SUBJECT MATTER

24. Claims 1-29 are allowed.

The following is an **Examiner's Statement of Reasons for Allowance**, **See MPEP 1302.14**:

25. The primary reason for allowance of claim 1 in the instant application is the combination with the inclusion in the claim that there are "**...A switch coupled between a plurality of host units and a device for routing frame information therebetween and comprising:**

a. a first serial advanced technology attachment (SATA) port including a first host task file responsive to a non-data frame information structure (FIS) from a first host unit;

b. a second SATA port including a second host task file, responsive to a non-data FIS from a second host unit;

c. a third SATA port including a device task file responsive to a non-data FIS from a device, the device supports queuing of the non-data FIS sent by the first and second host units and generates an original queue depth value indicative of a number of commands that the device can queue from either of the first or second host units; and

d. an arbitration and control circuit coupled to said first host task file and said second host task file and said device task file for selecting one of the first host or second host units to concurrently access the device, through the switch, by accepting the non-data FIS from either of the first or second host units, at any given time, including when the device is not in an idle state and whenever either one of the first or second host units sends the non-data FIS to the device, and further wherein the non-data FIS of the first and second host units and the device identify which one of the first or second host units is an origin or destination host

so that routing of the non-data FIS from the first and second host units and the device is transparent to the switch thereby reducing the complexity of the design of the switch rendering the switch's manufacturing less expensive, the arbitration and control circuit being responsive to the original queue depth value and alters the original queue depth value to be a new queue depth value that is less than the original queue depth value so that each of the first and second host units is assigned less than the number of commands indicated by the original queue depth value but that a total number of commands queued by the first and second host units remains the same as the original queue depth value thereby misrepresenting the original queue depth value to the first and second host units to be less than the original queue depth value thereby preventing the non-data FIS sent by the first and second host units from being lost by an overrun of the original queue depth value by either of the first or second host units ..." The prior art of record including the disclosures of Grieff et al. (US Patent 6,961,813), Utsunomiya et al. (US Pub.: 2003/0131166), Ooi et al. (US Patent 6,854,045) and Ooi et al. (US Patent 6,961,787) neither anticipates nor renders obvious the above recited combination. Because claims 2-8 and 21-23 depend directly or indirectly on claim 1, these claims are considered allowable for at least the same reasons noted above.

26. The primary reason for allowance of claim 9 in the instant application is the combination with the inclusion in the claim that there are "**... A switch comprising:**

a. a first serial advanced technology attachment SATA port including a first host task file for connection to a first host unit, said first SATA port responsive to a non-data frame information structure (FIS) from the first host unit;

b. a second SATA port including a second host task file for connection to a second host unit responsive to a non-data FIS from the second host unit;

c. a third SATA port including a device task file responsive to a non-data FIS from a device, for connection to the device, the switch for routing frame information between the first and second host units and the device, the device supports queuing of the non-data FIS sent by the first and second host units and generates an original queue depth value indicative of a number of commands that the device can queue from either of the first or second host units; and

d. an arbitration and control circuit coupled to said first host task file, said second host task file, and said device task file for selecting either the first host unit or the second host unit to concurrently access the device, through the switch, by accepting the non-data FIS from either of the first or second host units, at any given time, including when the device is not in an idle state, when either one of the first or second host units sends the corresponding non-data FIS to the device,

wherein while one of the first or second host units is coupled to the device, through the switch, the other one of the first or second host units sends the non-data FIS to the switch for routing to the device, and further wherein the non-data FIS from the first and second host units and the device identify which one of the

first or second host units is an origin or destination host so that routing of the non-data FIS from the first and second host units and the device is transparent to the switch thereby reducing the complexity of the design of the switch rendering the switch's manufacturing less expensive, further wherein the arbitration and control circuit is responsive to the original queue depth value and alters the original queue depth value into a new queue depth value that is less than the original queue depth value so that each of the first and second host units is assigned less than the number of commands indicated by the original queue depth value but that a total number of commands queued by the first and second host units remains the same as the original queue depth value thereby misrepresenting the original queue depth value to the first and second host units to be less than the original queue depth value so as to avoid the non-data FIS sent by the first and second host units from being lost by overrun of the original queue depth value by either of the first or second host units ..." The prior art of record including the disclosures of Grieff et al. (US Patent 6,961,813), Utsunomiya et al. (US Pub.: 2003/0131166), Ooi et al. (US Patent 6,854,045) and Ooi et al. (US Patent 6,961,787) neither anticipates nor renders obvious the above recited combination. Because claims 10-13 and 24-26 depend directly or indirectly on claim 9, these claims are considered allowable for at least the same reasons noted above.

27. The primary reason for allowance of claim 14 in the instant application is the combination with the inclusion in the claim that there are "**... A switch that is**

connectable to a first host unit, a second host unit and a device via serial advanced technology attachment (SATA) links, for routing frame information between the first and second host units and the device, said switch comprising:

a. a first SATA port, including a first host task file for connection to a first host unit, said first SATA port responsive to a non-data frame information structure (FIS) from the first host unit;

b. a second SATA port, including a second host task file for connection to a second host unit, responsive to a non-data FIS from the second host unit;

c. a third SATA port including a device task file responsive to a non-data FIS from a device, for connection to the device, the device supports queuing of the non-data FIS sent by the first and second host units and generates an original queue depth value indicative of a number of commands that the device can queue from either of the first or second host units;

d. an arbitration and control circuit coupled to said first host task file, said second host task file, and said device task file for selecting one of the first or second host units to concurrently access the device through the switch, by accepting the non-data FIS from either of the first or second host units, at any given time, including when the device is not in an idle state, when either the first or second host units sends the non-data FIS to the device,

wherein while one of the first or second host units is coupled to the device, the other one of to the first or second host units sends the non-data FIS to the switch for routing to the device, and further wherein the non-data FIS from the

first and second host units and the device identify which one of the first or second host units is an origin or destination host so that routing of the non-data FIS from the first and second host units and the device is transparent to the switch thereby reducing the complexity of the design of the switch rendering the switch's manufacturing less expensive,

further wherein, the arbitration and control circuit responsive to the original queue depth value and alters the original queue depth value into a new queue depth value that is less than the original queue depth value so that each of the first and second host units is assigned a new number of commands that is less than the number of commands indicated by the original queue depth value but that a total number of commands queued by the first and second host units remains the same as the original queue depth value thereby misrepresenting the original queue depth value to the first and second host units to be less than the original queue depth value thereby preventing the non-data FIS sent by the first and second host units from being lost by an overrun of the original queue depth value by either of the first or second host units ..." The prior art of record including the disclosures of Grieff et al. (US Patent 6,961,813), Utsunomiya et al. (US Pub.: 2003/0131166), Ooi et al. (US Patent 6,854,045) and Ooi et al. (US Patent 6,961,787) neither anticipates nor renders obvious the above recited combination. Because claims 15-18 and 27-29 depend directly or indirectly on claim 14, these claims are considered allowable for at least the same reasons noted above.

28. The primary reason for allowance of claim 19 in the instant application is the combination with the inclusion in the claim that there are "**...A method for communication between multiple host units and a device, through a serial advanced technology attachment (SATA) switch coupled to the multiple host units and the device using serial ATA links routing frame information therebetween comprising:**

a. receiving a non-data frame information structure (FIS) through a first SATA port including a first host task file, from a first host unit;

b. receiving a non-data FIS, through a second SATA port including a second host task file, from a second host unit;

c. receiving a non-data FIS through a third SATA port including a device task file;

d. arbitrating by an arbitration and control circuit between the first and second host units and the device;

e. selecting by the arbitration and control circuit one of the first or second host units to concurrently access the device through the switch, by accepting the non-data FIS, through the first and second host task files, from either of the first or second host units, when either of the first or second host units sends the non-data FIS for execution by the device;

f. coupling by the arbitration and control circuit the device to the selected one of the first or second host units;

g. while the selected one of the first or second host units is coupled to the device, the other one of the first or second host units sending the non-data FIS to the switch for routing to the device

during the sending step g., the non-data FIS of the first and second host units and the device identifying which one of the first or second host units is an origin or destination host so that the routing of the non-data FIS from the first and second host units and the device is transparent to the switch thereby reducing the complexity of the design of the switch rendering the switch's manufacturing less expensive;

h. intercepting by the arbitration and control circuit an original queue depth value generated by the device, the queue depth value being indicative of a number of commands that the device can queue from either of the first or second host units;

i. altering the original queue depth value by the arbitration and control circuit to be a new queue depth value that is less than the original queue depth value so that each of the first and second host units is assigned less than the number of commands indicated by the original queue depth value but that a total number of commands queued by the first and second host units remains the same as the original queue depth value thereby misrepresenting the original queue depth value to the first and second host units to be less than the original queue depth value thereby avoiding the non-data FIS sent by the first and second host units from being lost by overrun of the original queue depth value by either

of the first or second host units..." The prior art of record including the disclosures of Grieff et al. (US Patent 6,961,813), Utsunomiya et al. (US Pub.: 2003/0131166), Ooi et al. (US Patent 6,854,045) and Ooi et al. (US Patent 6,961,787) neither anticipates nor renders obvious the above recited combination. Because claim 20 depend directly on claim 19, claim 20 is considered allowable for at least the same reasons noted above.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/C.K.L./

December 05, 2008

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